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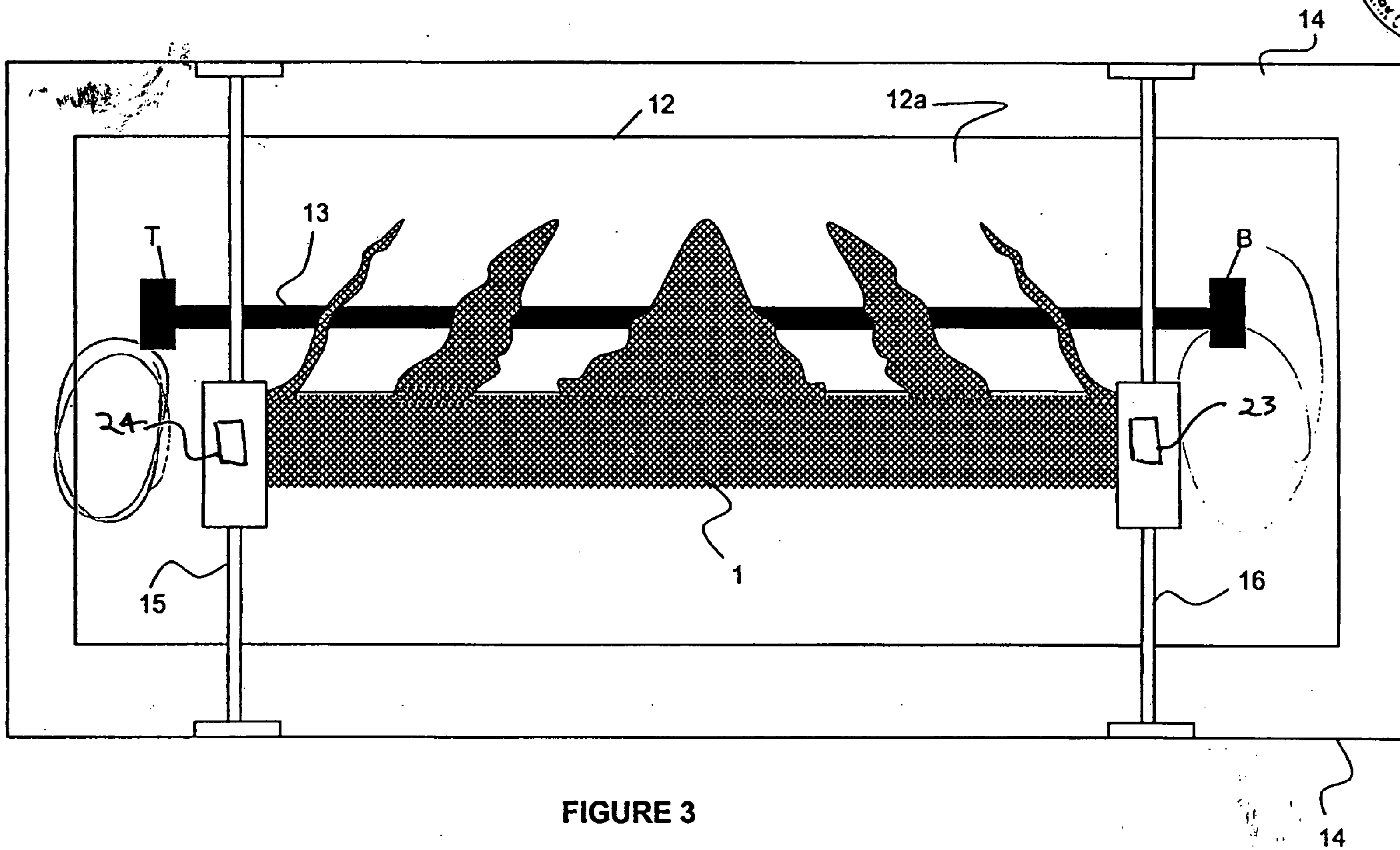

FIGURE 3

was written by Herman Chui at Stanford University. Because of the large energy sub-band splittings found, all of the carriers are assumed to lie in the first energy state. These are shown schematically in Fig. 5.7 for various Si thicknesses. To enter this information into SEDAN, which does not allow for multiple sub-bands, an "effective" conduction band offset for the surface Si layer was used to determine the position of the conduction band minimum. This effective offset was defined to be the potential difference between the relaxed-$Si_{0.7}Ge_{0.3}$ conduction band minimum, and the ground energy state in the surface Si layer, as shown in Fig. 5.7.

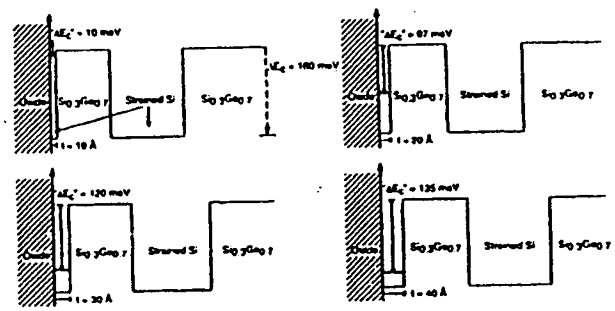

Figure 5.7 Band diagrams for dual strained-Si channel n-MOSFETs, indicating "effective conduction band offsets" due to quantization in the surface-Si layer.

The simulated carrier concentrations in each layer as a function of gate voltage are shown in Fig. 5.8. As the surface Si layer becomes thicker, it begins to invert at correspondingly lower gate voltages. This threshold shift is expected, since the effective conduction band minimum is moving to lower potentials with increasing well thickness. Because the surface Si channel inverts at lower gate voltages, the buried Si channel is screened more rapidly, so less carriers populate this channel. The result is that as the surface Si channel gets thicker, it dominates the device behavior over a larger voltage range. Above a certain thickness (on the order of 50 Å according to the simulations), it will completely dominate the behavior, and the device will appear to be almost identical to a surface-strained-Si n-MOSFET.

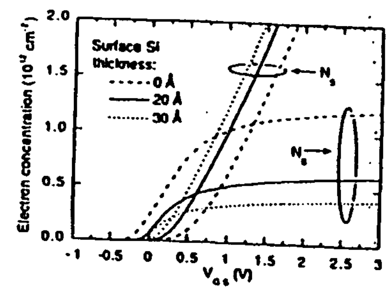

Figure 5.8 Calculated electron concentrations in a dual-channel n-MOSFET with various thicknesses of Si on the surface. The concentrations N_S and N_B are for the surface and buried strained-Si channels, respectively.

The measured field-effect mobility for several dual, strained-Si channel devices with various thicknesses of surface Si is shown in Fig. 5.9. Micro-Auger spectroscopy [109] was used to measure the Ge profile at the surface of each of these devices. This technique has a thickness resolution of about ± 5 Å. Since the layer thicknesses vary across the wafer, the spectroscopy was done directly on each device after electrical characterization. Variation in layer thicknesses across a single device was found to be less than the measurement resolution. Note that the underlying $Si_{0.7}Ge_{0.3}$ barrier layer, as well as the buried Si layer, showed differences in thickness between devices on the order of that measured for the surface Si layer. Simulation, however, indicates that the effect of these thickness variations on the carrier concentrations is small compared to the variation in the surface layer thickness.

Looking at each mobility curve in Fig. 5.9 individually, we can judge the effect of the surface Si layer. The device with < 5 Å of surface Si (t = 0 Å) was characterized in the previous section, and exhibits a large mobility peak at low gate voltage. This peak was correlated with transport in the high mobility, buried strained-Si layer, while the low mobility at higher gate fields was associated with parallel conduction in the low mobility, relaxed-$Si_{0.7}Ge_{0.3}$ layer on the surface. For the device with 10 Å of surface Si, the initial mobility peak is lower. This behavior is correlated to the lower threshold, and hence earlier turn-on, of the parallel surface channel, now that strained-Si is present be-

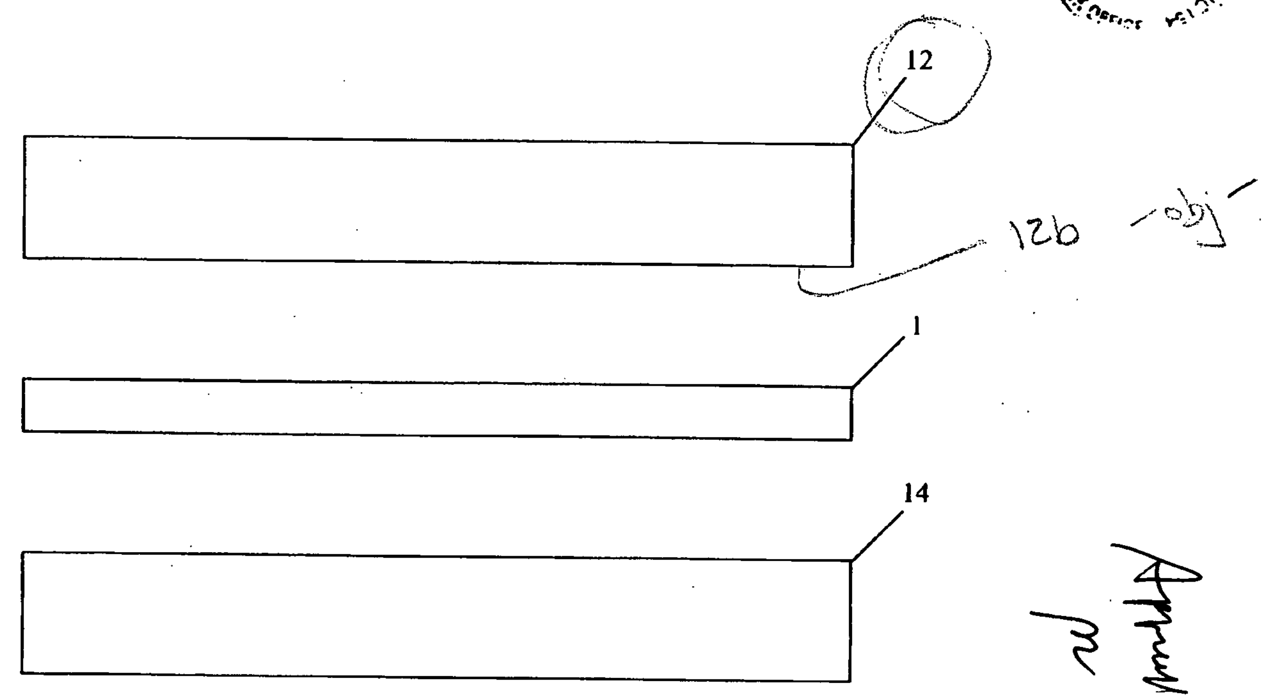

FIGURE 8

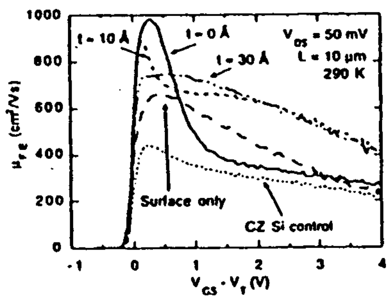

Figure 5.9 Field-effect mobility for dual-channel n-MOSFETs. The thickness t of the strained-Si on the surface of the device is indicated on the graph. Also shown are a device with only a single strained-Si layer on the surface (no buried layer) and a CZ Si control device for comparison.

low the oxide. The mobility at high gate fields, however, is significantly higher than what is measured in the purely buried device. This is not unexpected, since the mobility in the strained-Si at the surface is expected to be higher than that of relaxed $Si_{0.7}Ge_{0.3}$. In addition, there may be some improvement in the oxide interface quality since the interface is now further separated from the $Si_{0.7}Ge_{0.3}$ interface [111], which would also improve the mobility in the surface layer. The device with 30 Å of surface Si continues this behavior trend. Now, there is no discernible initial peak in the mobility, but the mobility at higher gate fields remains high, giving a flat mobility profile that appears very similar to a surface channel device.

In addition to the mobility from a CZ Si control n-MOSFET, the field-effect mobility for a surface channel, strained-Si device is also shown in Fig. 5.9 for comparison to the dual-channel devices. This device (shown in Fig. 4.1(a)) has a single strained-Si channel directly below the oxide, which is similar to the surface channel in the dual-channel devices, but somewhat thicker (≈ 100 Å). The mobility from this device shows no large peak, and is expected to be similar in magnitude to that of the surface channel in each of the dual-channel devices. As seen in the figure, it is lower than the overall mobility extracted for the dual-channel devices, perhaps because their mobility

includes a high mobility component from the carriers in the buried channel. For thicker layers of surface Si layer, the dual-channel devices begin to appear more and more like the pure surface channel device, as the surface channel dominates the buried channel. Optimization of the relative thickness of the two channels might be possible, trading off a high mobility peak at low gate voltages for a higher overall mobility over a larger voltage range. As discussed in the previous section, direct comparison between surface and buried channel devices is difficult, but the qualitative explanation given here correlates well with the observed behaviors.

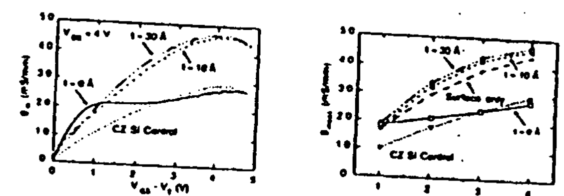

Figure 5.10 Transconductance behavior of dual-channel n-MOSFETs. The peak g_{msat} for the devices is shown for various values of V_{DS}, illustrating how the relative thickness of the channels changes the device performance in different voltage ranges. (L = 10 µm)

A similar performance trend can be seen in the transconductance of the devices. As shown in Fig. 5.10, at low gate voltages, the device with no measurable surface Si has the highest transconductance, but this drops off rapidly. At higher gate fields, the devices with thin layers of Si on the surface exhibit a higher transconductance, since the high mobility material on the surface extends the range of the performance enhancements. Again, the surface-only strained-Si device shows a slightly lower g_{msat} performance compared to the dual channel devices, perhaps due to the absence of a high-mobility parallel, buried channel.